CLAIMS

What is claimed is:

1. A low-jitter clock distribution circuit, comprising:

5   a plurality of cascaded inverters, each inverter including an upper P-channel transistor connected to a lower N-channel transistor, the channel lengths of the P-channel and N-channel transistors in each inverter being substantially equal, the ratio Wp/Wn of the widths of the P-channel and N-channel transistors in

10   each inverter being equal to substantially the square root of the ratio Un/Up of the majority carrier mobilities of the N-channel and P-channel transistors as determined by a semiconductor fabrication process by which the clock distribution circuit is manufactured.

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2. A low-jitter clock distribution circuit according to claim 1, wherein the ratio of Wp/Wn in each inverter is within the range of +/- about 25% of the square root of the ratio Un/Up.

20   3. A multiple-channel analog-to-digital converter integrated circuit, comprising:

      a plurality of analog-to-digital converters, each analog-to-digital converter having a clock input for receiving a sampling clock; and

25   a clock distribution circuit for distributing a clock signal to the clock input of the analog-to-digital converters, the clock distribution circuit including a plurality of cascaded inverters, each inverter including an upper P-channel transistor connected to a lower N-channel transistor, the channel lengths of the P-channel

30   and N-channel transistors in each inverter being substantially equal, the ratio Wp/Wn of the widths of the P-channel and N-channel transistors in each inverter being equal to substantially the square root of the ratio Un/Up of the majority

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carrier mobilities of the N-channel and P-channel transistors as determined by a semiconductor fabrication process by which the integrated circuit is manufactured.

5   4. A multiple-channel analog-to-digital converter integrated circuit according to claim 3, wherein the ratio of Wp/Wn in each inverter is within the range of +/- about 25% of the square root of the ratio of Un/Up.

10   5. A low-jitter clock distribution circuit, comprising:
        a plurality of cascaded inverters, each inverter including an upper P-channel transistor connected to a lower N-channel transistor, the channel lengths Lp and Ln of the P-channel and N-channel transistors in each inverter being unequal, the
15   N-channel and P-channel transistors having a ratio Un/Up of majority carrier mobilities as determined by a semiconductor fabrication process by which the clock distribution circuit is manufactured, the ratio Wp/Wn of the widths of the P-channel and N-channel transistors in each inverter being equal to
20   substantially the square root of (Un/Up*Lp/Ln*(A*Ln + 1)/(A*Lp + 1)), where A is a parameter determined by the semiconductor process.

6. A low-jitter clock distribution circuit according to claim 5,
25   wherein the ratio of Wp/Wn in each inverter is within the range of +/- about 25% of the square root of (Un/Up*Lp/Ln*(A*Ln + 1)/(A*Lp + 1)).

7. A multiple-channel analog-to-digital converter integrated
30   circuit, comprising:
        a plurality of analog-to-digital converters, each analog-to-digital converter having a clock input for receiving a sampling clock; and

a clock distribution circuit for distributing a clock signal to the clock input of the analog-to-digital converters, the clock distribution circuit including a plurality of cascaded inverters, each inverter including an upper P-channel transistor connected to a lower N-channel transistor, the channel lengths Lp and Ln of the P-channel and N-channel transistors in each inverter being unequal, the N-channel and P-channel transistors having a ratio Un/Up of majority carrier mobilities as determined by a semiconductor fabrication process by which the integrated circuit is manufactured, the ratio Wp/Wn of the widths of the P-channel and N-channel transistors in each inverter being equal to substantially the square root of (Un/Up*Lp/Ln*(A*Ln + 1)/(A*Lp + 1)), where A is a parameter determined by the semiconductor process.

8. A multiple-channel analog-to-digital converter integrated circuit according to claim 3, wherein the ratio of Wp/Wn in each inverter is within the range of +/- about 25% of the square root of (Un/Up*Lp/Ln*(A*Ln + 1)/(A*Lp + 1)).